MicroLok® II Central Processing Unit (CPU) PCBs: Standard, PTC-Upgradeable, VitalNet™ and Genisys® II CSIB

MicroLok II CPU PCBs perform all of the essential decision-making and communications functions of MicroLok II-based vital and non-vital systems. In addition, they permit on-site or remote access of the entire MicroLok II-controlled system for routine monitoring or diagnostic purposes. The CPU can also serve as a high-capacity wayside event recorder, simultaneously monitoring scores of parallel and serial I/O events (for example, at a complex interlocking), as well as its own operations. Thousands of CPU boards have been in successful service on mass transit lines and railroads around the world for nearly 15 years. In those 15 years, numerous hardware and software refinements have been applied, improving its original capabilities and reliability even further. The latest “VitalNet” advancement enables MicroLok II to function in Positive Train Control (PTC) applications.

Descriptions

Standard CPU PCB (N17061301 and N17061315)
The Standard MicroLok II CPU PCB performs a variety of functions such as:

- Monitoring external indications from vital input PCBs and non-vital input PCBs.
- Processing vital external indications and executing logic defined in the Application logic.
- Driving vital output PCBs as required by the Application logic.
- Monitoring and controlling serial communication ports (which are links to other controllers).

The CPU PCB is controlled by a 68332 microprocessor, which operates at a speed of 21MHz. Most internal operations are 32 bits wide. All outside bus cycles are 16 or 8 bits wide. The Executive and Application logic is stored in four flash Erasable Programmable Read-Only Memory (EPROM) chips that provide up to 8MB of memory. Flash EEPROMs permit direct handling of the software using a laptop Personal Computer (PC) connected to the CPU PCB front panel diagnostics serial port connector. Jumpers on the CPU PCB enable or disable the flash EEPROMs for programming and select programming voltage.

Two independent banks (128KB total) of fast Static Random-Access Memory (SRAM) are provided on the CPU PCB for processing vital data. Events and errors are stored in up to four 256KB banks of low power SRAM. Error/event memory is maintained by a capacitor backup that provides up to four hours of short-term Random Access Memory (RAM) protection. The CPU is also designed to store read/write data in one of two optional Personal Computer Memory Card International Association (PCMCIA) card slots, using a PCB-mounted cardholder. This additional memory is used to increase the on-board event recording capability. The CPU PCB uses a real time clock based on a 32.768MHz oscillator. The same capacitor and external lithium battery used for the fast SRAM also backup this device. The CPU PCB has five serial data ports, four of which are intended for communications with external vital and non-vital devices. The remaining port interfaces with a laptop PC, which connects to the front panel 9-pin connector.

Two alphanumeric displays on the CPU PCB display menus allowing the user to obtain system information without having to connect a laptop PC. The menus include two Reset (one for configurable devices and one for non-configurable devices) and an On-Line menu.

The “315” version of the Standard CPU PCB is European CENELEC-certified.
PTC-Upgradeable CPU PCB (N17067601)
This CPU PCB is fully backward-compatible with the Standard CPU PCB (see above description) and is designed to be upgraded (when required) to Positive Train Control (PTC) functionality using the VitalNet Co-Processor Daughter PCB (see following description).

The basic “601” PCB incorporates uses much of the same hardware as the “301” PCB above, including four external-system serial ports and one front panel laptop-compatible port. See diagram at right for the front panel layout. The “601” PCB can be used with all ASTS USA I/O bus and modular-based products such as End-Point, Half-Box and Intermediate.

VitalNet CPU PCB (N17067602)
The VitalNet CPU PCB is comprised of the PTC-Upgradeable CPU (see previous section) and the VitalNet Co-Processor Daughter PCB, which is attached to it. The combined assembly is referred to as the MicroLok II VitalNet™ CPU. This combined PCB assembly enables integrated Positive Train Control (PTC) Wayside Interface Unit (WIU) functionality in within a MicroLok II-based interlocking control system.

The board transfers vital interlocking data messages, containing wayside signal indications, switch positions and hazard indicator statuses to a radio that forwards it to the carborne ATP equipment on approaching vehicles. It monitors the states of the wayside devices and vitally constructs a message that depicts those states. Each message is delivered to a Wayside Communications Module (WCM) that chooses the most appropriate media to send the message to a train.

VitalNet Co-Processor Daughter PCB
MicroLok® II Central Processing Unit (CPU)  
PCBs: Standard, PTC-Upgradeable,  
VitalNet™ and Genisys® II CSIB  

Descriptions (cont’d)  

VitalNet CPU PCB (N17067602) (cont’d)  
The VitalNet Co-Processor Daughter PCB communicates with the main CPU through a vital communications protocol. Two diverse Field-Programmable Gate Arrays (FPGAs) to implement a 2-out-of-2 voting architecture, which provides vital reception of MicroLok II input and output states, and vital generation and transmission of PTC messages to the data radio or back office.  
The VitalNet system contains two independent and isolated Ethernet connections through RJ-45 connectors on the front panel of the PCB. These ports may be used simultaneously. They are intended for use with the WCM to exchange messages with the train, and to respond to inquiries from the central office. Additionally, the Ethernet ports can be used for maintenance functions. The ports may be configured as DHCP clients for connection to a WCM or existing IP network, or may be configured to serve as DHCP hosts for maintenance functions without the need to change Network settings on the maintainer’s PC.  
The VitalNet Co-processor contains an embedded web server interface so that a user can connect a laptop PC to the Ethernet port to configure the device, modify the PTC application settings, upload and download software, and view diagnostic and event data. In addition to Executive and Application software, the VitalNet CPU PCB is programmed with location-specific PTC application and configuration software.

Genisys II Code System Interface PCB (N17061302)  
The Genisys II Code System Interface Board (CSIB) is an enhanced replacement for the Genisys 2000-based CSIB (N17061401). The new CSIB functions as an interface between various non-vital code line protocols commonly used in the railroad industry. It is physically identical to the standard N17061301 CPU, having the same front panel layout, connector pinouts and option jumpers. The CSIB operates using the non-vital Genisys II Executive software, which is structurally similar to the MicroLok II vital Executive.  
When the “302” CPU is used exclusively in a non-vital MicroLok II application, it supports all of the non-vital MicroLok II I/O boards (refer to RSE-1D2.3). However, it is not capable of controlling the vital MicroLok II I/O boards. The Genisys II CSIB is supported by the Genisys II Development System, which is similar to the MicroLok II Development system.  
Note: This CSIB is not a direct replacement for the Genisys 2000-based PCB N17061401. Connector rewiring is required to install the newer PCB.

Advantages  
- CPUs provide comprehensive monitoring and control of vital or non-vital MicroLok II systems.  
- Perform continuous internal and external diagnostics to ensure system reliability and safety.  
- Ample memory available to perform as a wayside event recorder.  
- Four serial ports compatible with a variety of communications architectures.  
- Easily accessed (on-site or remote) to check/download event logs and perform diagnostics.  
- VitalNet versions meets requirements for the latest PTC standards and applications.  
- VitalNet Co-Processor (Embedded Web Server Interface) Features:  
  - Enables connection of laptop PC via Ethernet port  
  - Device configuration  
  - Modify PTC application settings  
  - Upload/download software  
  - View diagnostic and event data  
- Genisys-II version accommodates all of the railroad code system applications of the earlier “401” CSIB.

Specifications  
Standard PCBs “301”, “302” and “315”  
Microprocessor Type: 68322  
Microprocessor Speed: 21 MHz  
Operations:  
  - Internal: 32 bits wide  
  - Outside bus: 8 or 16 bits  
Flash Memory:  
  - Flash EPROMs: 4  
  - Capacity: Up to 8MB  
PCMCIA Cards:  
  - 1 or 2. Additional memory: Up to 8MB (4M x 16)  
  - Programming voltages: +5V and +12V  
Vital Data Processing:  
  - Fast SRAM: 2 banks  
  - 128 KB (total)  
Event/Error Storage:  
  - Low-power SRAM: Up to 4 banks, 256 KB (each)  
  - Protection: Up to 4 hours RAM
MicroLok® II Central Processing Unit (CPU)
PCBs: Standard, PTC-Upgradeable, VitalNet™ and Genisys® II CSIB

Specifications (cont’d)

PTC-Compatible/VitalNet PCBs “601” and “602”

Microprocessor: MC68322 (32-bit)
2KB internal fast-termination RAM

Operations: Internal: 32 bits wide
Outside bus: 8 or 16 bits

Independent Clock: 2MHz (enable)
Supports older 6800 peripherals

Flash Memory: Flash EPROMs: 4
Capacity: Up to 8MB

PCMCIA Cards: 1 or 2
Additional memory: Up to 8MB (4M x 16)

Vital Data Processing: Fast SRAM: 2 banks
128 KB (total)

Event/Error Storage: Low-power SRAM: Up to 4 banks
256 KB (each)
Protection: Up to 8 hours RAM

Serial Ports: Four external: Two RS-485, two RS-232
One front panel: One RS-232

VitalNet Co-Processor Daughter PCB (PTC Applications)

Mounting: 6 PCB stand-offs
Daughter-to-CPU Link: Vital protocol

ASTS USA G96 Bus
Two diverse FPGAs
2-out-of-2 (2oo2) voting

Ethernet Connections: Independent/isolated
RJ-45 connectors

Ethernet Configuration: Options:
DHCP clients for WCM or existing IP network
DHCP host for maintenance functions

Genisys CSIB PCB

Hardware: Identical to Standard CPU
Code System Protocols: Genisys Master
Enhanced Genisys Slave
MicroLok II Peer Protocol
Enhanced SCS-128 Slave
Enhanced MCS-1 Slave
ARES WIU
ATCS WIU
GETS Serial Local Control Panel (SLCP)
S2 Slave

Ordering and Additional Information

- Refer to tabulation for CPU-based PCBs’ part numbers.
- Contact your ASTS USA Account Executive for CPU PCB software updates and MicroLok II applications possibilities in general.
- Request the following ASTS USA Service Manuals for additional information:
  - Standard CPU PCB: SM-6800A, -B, -C, -D
  - PTC-upgradeable CPU: SM-1D1.0028
  - VitalNet Co-Processor Daughter PCB: SM-1D1.0031
  - Genisys II CSIB: SM-6800M

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